ABSTRACT OF THE DISCLOSURE

A system and method for transferring data from circuitry disposed in a higher frequency clock domain actuated by a first clock signal to circuitry disposed in a lower frequency clock domain actuated by a second clock signal, wherein the first and second clock signals are provided in a predetermined frequency ratio. A first latch gated by a first modified clock signal that is derived from the first clock signal and plurality of intermediary signals relating thereto is operable to generate a first latched data output, which is provided to a second latch disposed in the lower frequency clock domain. The second latch gated by a second modified clock signal that is synthesized using the second clock signal and at least one intermediary clock signal derived therefrom is operable to generate a second latched output. A register is operable to synchronize the second latched data output into a synchronized data output for subsequent use by the circuitry disposed in the lower clock frequency domain.